Utilizing Thermal Fatigue Testing to Differentiate the Performance of Epoxy Materials at Various Glass Transition Temperature Levels

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Abstract
A common method for understanding the thermal performance of epoxy laminate materials is to analyze the glass transition temperature using instruments such as Differential Scanning Calorimetry (DSC), Dynamic Mechanical Analysis (DMA) and Thermomechanical Analysis (TMA). In order to characterize the long-term performance of a finished printed circuit board, more advanced reliable test methods have been developed. This paper will discuss Interconnect Stress Testing (IST), an accelerated fatigue test used for evaluating the failure modes of a printed circuit board (PCB) interconnect. IST utilizes a DC current to heat the PCB to the recommended temperatures within the interconnect. The plated through hole integrity and the post interconnect integrity can be monitored simultaneously. The test matrix compares the performance of various AlliedSignal epoxy laminate materials as a function of glass transition temperature (Tg) and board design.

Introduction
Due to the increasing demands in the electronics industry, the need to analyze and understand the long-term performance of the printed circuit board is becoming more significant. Data on the thermal performance of printed circuit boards is usually published as a means of glass transition temperature (Tg). Glass transition temperatures can be measured efficiently via Differential Scanning Calorimetry (DSC), Dynamic Mechanical Analysis (DMA) or Thermomechanical Analysis (TMA). The question still remains, however, what the correlation of glass transition temperature is to the thermal integrity of a printed circuit board.

Thermal cycle testing is a method that characterizes the thermal integrity of a finished board. The purpose of thermal cycle testing is to determine how well the printed circuit board can withstand various temperature extremes. Although difficult to illustrate every board design, test vehicles can focus on plated through holes, which is a key factor in typical designs and is also the area that is most susceptible to failure when subjected to thermal cycle testing. The integrity of the test coupons can be determined by the resistance measurement from one end of the circuit to the other. Through the progression of each thermal cycle, stresses are induced at the plated through hole. This results in a breakdown of the printed circuit board integrity due to barrel or hole wall cracks in the copper circuit. As the cracks propagate, the resistance of the circuit will increase. The mode of failure, since not always detrimental, is determined as a percent increase in resistance from the initial resistance measurement.

Test methods for thermal cycling commonly utilize mediums for heat transfer such as air or a silicone liquid. A more recent accelerated fatigue test, Interconnect Stress Testing (IST), is emerging as a future test method for quantifying the integrity of the printed circuit board. IST is an automated method in which a DC current is passed through a circuit. The temperature of the copper at the plated through hole as well as at the interconnecting track cycles from ambient to a temperature which approaches the glass transition temperature of the laminate material. During each thermal excursion, the resistance is monitored and the point at which the defect begins to develop as well as the point at which failure can be detected.

Test Vehicle Design
In an effort to correlate glass transition temperature to the long-term performance of a circuit board by means of thermal cycling, variables that could potentially cause premature failure were eliminated from this test. All of the coupons were tested from a ten-layer board construction utilizing the same laminate and prepreg material combinations. Panels were processed through plating simultaneously. The coupons subjected to IST were removed from the same location on each panel [which has been an influencing factor on thermal cycling results in the past[1]].

Test coupons were prescreened to determine the most consistent plating. The coupons of similar plating consistency were selected from panels of FR-4 epoxy laminate materials with different glass transition temperatures. AlliedSignal Laminate

Systems designed the multilayer test vehicle used for this evaluation. Four different FR-4 epoxy laminate materials with glass transition temperatures of 135°C, 140°C, 150°C and 170°C were investigated. The ten-layer coupons were built from test panels of a 24”x18” circuit area, laminated to 0.084”. Each test coupon consisted of two daisy-chained circuits, finished with either a 0.040” or 0.0135” hole size. Each hole size consisted of plated through holes with non-functional pads on all layers or the removal of all non-functional pads. Innerlayers were produced with one ounce copper foil. The ten-layer boards were processed with electroless copper and finished with tin/lead (HASL). The coupons consisted of two independent circuits for both hole sizes and internal pad configuration: the plated through hole interconnect and the post interconnect circuit. Post interconnect circuits were positioned on two adjacent internal layers (i.e. 2 and 3). The post interconnect circuit is utilized for measuring print and etch variability as well as passing the DC current through the coupon for IST temperature control. The plated through hole circuits were positioned on two internal layers and two external layers. This daisy chain pattern interconnects the vias from top to bottom and from external to internal layers. This circuit is utilized to monitor crack propagation as well as in-plane separations or foil cracking. The plating thickness variability and the plated through hole degradation are determined by the plated through hole circuit during Interconnect Stress Testing. All test coupons were prescreened to determine the bulk resistance variability.

Prescreening Results

Electrolytic copper plating causes differences in resistance levels/plating distributions. Due to the influence that plating thickness has with regards to the performance of the base material, prescreening was conducted on every test coupon to determine the most consistent plating thickness for each material grade. Each panel was mapped according to panel plating distribution relative to resistance. (See Figure 1-4). The resistance was graphed with respect to the coupon location (A1, B1, C1, and D1) of the board (left, middle, and right). The plating relative to resistance levels was analyzed at every location on the board to determine which coupons were the most consistent compared with the coupons constructed with different material types at the same location. Statistical correlation coefficients were utilized to determine the consistency of the copper plating in each of the identified panels. The individual resistance maps in conjunction with the correlation coefficients determined the levels of consistency between test panels of every grade. The criterion for panel selection was based on the minimal resistance/plating thickness variance of each grade of material. The test coupons showing the most consistent results from the same location of these selected panels were chosen for interconnect stress testing.

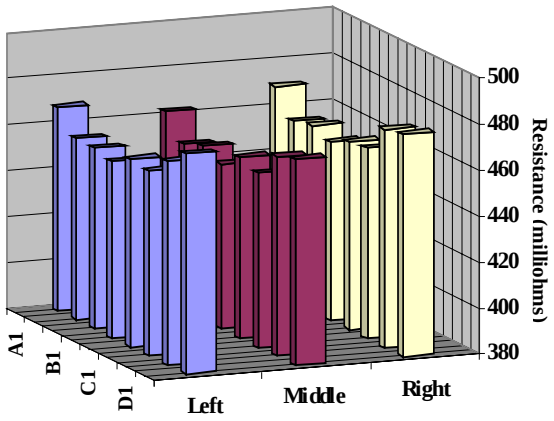
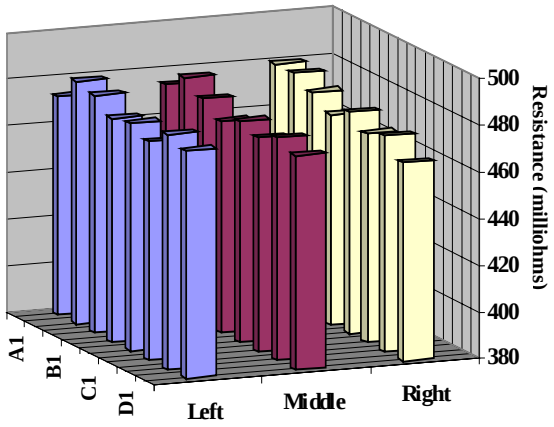


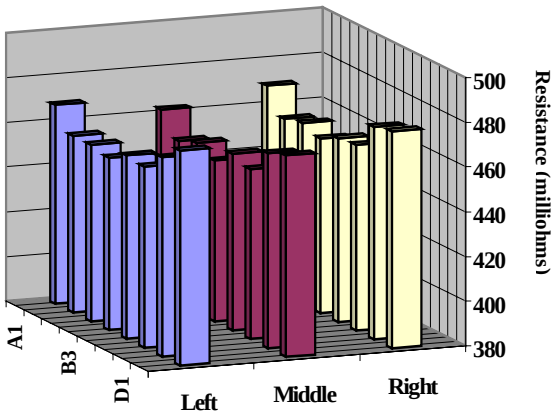
Figure 1 - A resistance map of the 135°C Tg FR-4 epoxy laminate material

Figure 2 - A resistance map of the 140°C Tg



FR-4 epoxy laminate material

Figure 3 - A resistance map of the 150°C Tg



FR-4 epoxy laminate material

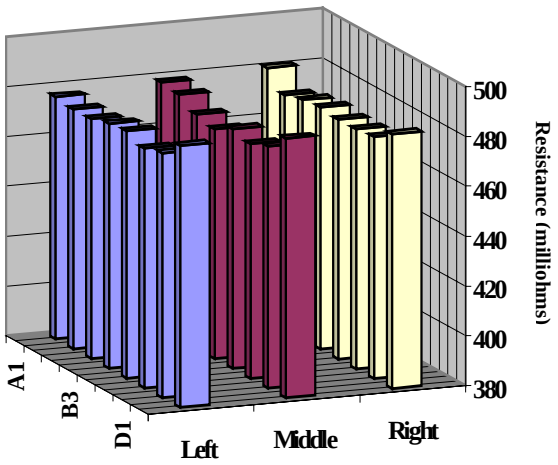


Figure 4 - A resistance map of the 170°C Tg FR-4 epoxy laminate material

Test Procedure

A predetermined constant DC current is passed through the selected test coupons. The current elevates the temperature of the test coupon to a level near the glass transition temperature. There is a mathematical relationship which defines the correlation of the interconnect temperature to the amount of current being passed through. The temperature of the heated coupon is directly proportional to the measured resistance and the amount of current that is passed through the conductors, pads, and holes. The IST system raises the temperature of the interconnect to a predefined level. When that level is reached, the IST system turns off this current. The coupons remain in the heated stage for three minutes and then are cooled by forced air for two minutes, which takes the temperature back to ambient levels. This exemplifies a single IST thermal cycle.

As the thermal excursions progress, the system continuously monitors any resistance changes in the plated through hole and the innerlayer to post interconnect. The system automatically repeats the thermal cycles until failure has been attained. A predetermined failure criterion is determined which is a 10% increase in resistance relative to the initial resistance measurement. An increase in resistance up to 10% is significant to reveal the crack propagation around the interconnects.[2]

IST Test Results

The IST cycles to failure results, including each hole size and pad configuration, are shown in Figure 5 and Figure 6. The resistance changes were continually monitored in both the plated through hole and post interconnects throughout IST. In both figures, the failure mode was recognized as the point at which a 10% increase in resistance occurred from the initial resistance measurement.

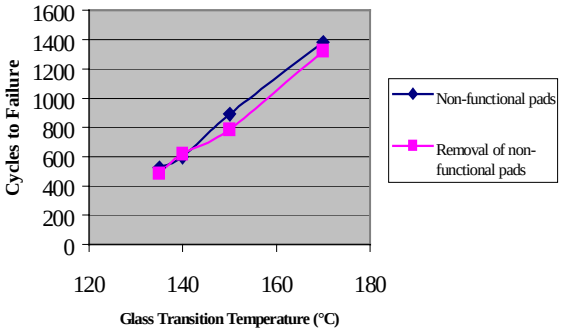


Figure 5 - IST Results (0.040" diameter holes)

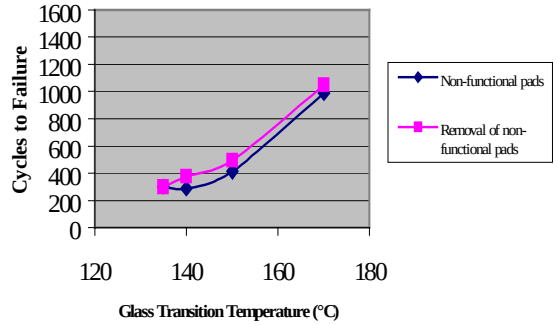


Figure 6 - IST Results (0.0135" diameter holes)

Discussion

The IST results show the impact of internal pads, which can cause long-term detrimental effects on interconnect performance. However, this is influenced by the combination of the material type and hole diameter. The IST cycles to failure on the coupons with 0.040" vias showed the internal pads, in most of the material types, negatively affecting the performance up to 12%. As the aspect ratio increases, by a change in the hole diameter for example, the impact of internal pads positively influences the performance as much as 20% relative to the material type. The impact of the internal pads, positively or negatively, is dependent on the material type.

It was determined that plated through hole fatigue was the dominant failure mechanism. This type of fatigue was caused by strains which created cylindrical barrel cracking in the plated through holes. Microsectioning was performed to illustrate the barrel cracking, shown in Figures 7 and Figure 8. Microsection analysis and Interconnect Stress Testing were run independently and the results were not compared until both sets of data were completed. IST in coordination with microsectioning is useful for rationalizing the printed circuit board

performance. Post interconnecting separations were not detected on any of the coupons during testing and failure analysis. Whether or not internal pads are utilized, the material type appears to show a significant effect on the interconnect performance. As the glass transition temperature increases, the IST cycles to failure linearly increases. As the aspect ratio increases, the improvement in the IST results relative to glass transition temperature becomes more significant.

Interconnect Stress Testing was performed by PWB Interconnect Solutions, Incorporated. The IST results were compared with historical data of similar technology levels and attributes. The IST cycles to failure results of the AlliedSignal materials were recognized as above the traditional baseline level relative to performance.

Studies have shown that premature failure can exist due to multiple variables, which can potentially skew the thermal cycling results. The potential variability was eliminated from board design to plating consistency of the coupons from the same location of the panel. From this study, the coupons were selected from the center of the panel revealing the most consistent plating from a panel of one material type to another material type.

Figure 7 - Microsection revealing cracks in the plated through hole

Conclusion

In order to distinguish the long-term performance of FR-4 epoxy laminate materials with different glass transition temperatures, appropriate measures need

Figure 8 - Microsection taking a closer look at the location of failure

to be taken in order to reduce any variability that could potentially cause premature failure. Coupon selection through prescreening for determining plating consistency was an example that reduced the degree of variability.

The innerlayer pad configuration and the drilled hole diameter were variables for identifying the influence of glass transition temperature on the long-term performance of a printed circuit board. The IST results showed an increasing trend of interconnect performance as the glass transition temperature increased. The pad configuration recognized the same trend but was heavily dependent on the material type as to being a positive or negative affect on the printed circuit board performance. As the hole diameter decreased, the results revealed a much more significant trend of the same nature. As the demands in the electronics industry are seeking changes in the aspect ratio, the glass transition temperature as correlated with the thermal performance of the circuit board will be a critical factor for ideal material selection.

References

[1] Coppens, Dave, “Using Thermal Shock to Compare Standard, Medium and High Temperature Epoxy Performance”, IPC Expo March 1998 Proceedings.

[2] IST Technology, PWB Interconnect Solutions Incorporated, P.O. Box 23022, Ontario, Canada, K2A 4E2.

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